REMARKS/ARGUMENTS

Claims 1-4, 7-11, 14, 15, 18, 19, 22, 23, and 26-36 are pending in the present application. Claims 1, 11, 15, 19, and 23 are amended. Claims 1, 11, 15, 19, and 23 are independent.

Interview on March 25, 2004

Applicants wish to thank Examiner David Odland and Primary Examiner John Pezzlo for taking the time to discuss the application with Applicants' Representative, Jason Rhodes, on March 25, 2004. Although no agreement was reached, Applicants have now gained a better understanding of the Examiner's position regarding the outstanding prior art rejections. The substance of this interview is provided below, in accordance with MPEP § 713.04.

Substance of the Interview

I) **Exhibit shown/demonstration conducted:**

No exhibit was shown and no demonstration was conducted during the interview.

II) **Claims Discussed:**

Independent claims 1 and 11 were discussed during the interview.

III) **Prior Art Discussed**:

U.S. Patent No. 4,924,464 to Baylock (hereinafter Baylock) was discussed.

IV) **Proposed Amendments**:

Applicants' Representative did not propose any specific claim amendments. However, the Primary Examiner suggested that the claims could be amended to distinguish over Baylock by reciting some specific use or advantage of converting the parallel signal into multiple serial signals.

V) **Principle Arguments**:

Applicants' Representative argued that the Baylock patent failed to disclose the insertion of stuffing data to received bits during parallel-to-serial conversion, as required by independent claims 1 and 11.

VI) **Other Pertinent Matters Discussed**:

As indicated above, the Primary Examiner suggested various types of amendments that may distinguish the present claims over Baylock.

VII) **General Results**:

No agreement was reached as to whether independent claims 1 and 11 presently distinguish over Baylock. However, Applicants' Representative agreed to consider the Primary Examiner's suggestion of amending the claims.

Claim Objections

Claim 1 is objected to because: 1) The claim recites that the receiving circuits receive bits over "output line" (line 5); and 2) the claim recites sending converted serial signals "to one or more corresponding transmission circuit" (lines 10 and 11). Applicants respectfully submit that line 5 of claim 1 has been amended to replace "output lines" with "input lines." As to the other grounds of the objection, Applicants respectfully submit that the claim actually recites sending the serial signals "to one or more corresponding transmission circuits" in lines 10-12, and no further amendment is needed.

Accordingly, Applicants respectfully request reconsideration and withdrawal of this objection.

Rejections Under 35 U.S.C. § 103

Claims 1-4, 7-11, 14, 15, 18, 19, 22, 23, and 26 stand rejected under 35 USC § 103(a) as being unpatentable over

Baylock in view of U.S. Patent No. 5,040,170 to Upp et al. (hereinafter Upp). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

As amended, each of independent claims 1, 11, and 19 recites converting a parallel signal into serial signals and transmitting the serial signals over a backplane, whereby the conversion of the parallel signal into serial signals allows the backplane to be less complex. Each of independent claims 15 and 23 recites receiving bits and serial signals from a backplane and converting the serial signals to a parallel signal, where the receiving of bits in serial signals allows the backplane to be less complex.

As discussed in the present specification (see, *inter alia*, page 12, line 20 through page 13, line 7), a communication device that transmits signals over a backplane to other devices can reduce the size of the backplane footprint required for connecting the device to the backplane. Specifically, it is known in the art that transmitting parallel signals (e.g., 8-bit signal) over a backplane would require a footprint through which a parallel bus (e.g., 8-bit wide) can connect the device to the backplane. By converting the parallel signal to serial signals before transmission, the device only requires a footprint through which a one-bit wide bus is connected to the backplane. Similar advantages can be obtained by devices that process data as parallel signals,

if the device is configured to receive the data from the backplane as a serial signal and convert it into a parallel signal.

Accordingly, exemplary embodiments of the present invention reduces the complexity of the backplane by converting parallel signals into serial signals before transmission over the backplane, and receiving data from the backplane of serial signals.

Applicants respectfully submit that neither Baylock nor Upp provide any teaching or suggestion of transmitting or receiving signals over a backplane, as required by independent claims 1, 11, 15, 19, and 23. Thus, Baylock and Upp do not teach or suggest reducing the complexity of a backplane. Since the prior art does not teach or suggest all of the claim limitations, as required by an obviousness rejection under 35 U.S.C. § 103(see MPEP § 2143.03), Applicants respectfully submit that the claims are allowable over the prior art at least for the reasons set forth above. Furthermore, Applicants submit that claims 2-4, 7-10, 14, 18, 22, and 26 are allowable at least by virtue of their dependency on claims 1, 11, 15, 19, and 23.

Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claims 27-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baylock in view of Upp, and further in view of

U.S. Patent No. 5,159,595 to Flanagan et al. (hereinafter Flanagan). Applicants respectfully submit that Flanagan fails to remedy the deficiencies of a Baylock and Upp set forth above in connection with independent claims 1, 11, 15, 19, and 23. Accordingly, Applicants submit that claims 27-31 are allowable at least by virtue of their dependency on claims 1, 11, 15, 19, and 23. Reconsideration and withdrawal of this rejections is, therefore, respectfully requested.

It is further respectfully submitted that the above amendments to the independent claims do not constitute an admission by Applicants as to the validity of the outstanding § 103 rejection over Baylock and Upp. It is still Applicants' position that Baylock fails to disclose the insertion of stuffing data during a process for converting a parallel signal into serial signals, and that Upp fails to remedy this deficiency in Baylock. However, Applicants have amended the claims in order to more clearly distinguish the claims and expedite prosecution in this application.

Conclusion

In view of the above amendments and remarks, the Examiner is respectfully requested to reconsider and withdrawal all

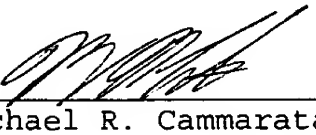
outstanding rejections. Applicants earnestly seek a Notice of Allowance in connection with the pending claims.

Should the Examiner believe that any outstanding matters remain in the present application, the Examiner is strongly encouraged to contact Jason W. Rhodes at the telephone number of the undersigned in order to conduct an interview in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By 
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